

REMARKS/ARGUMENTS

This application has been carefully reviewed in light of the Final Office Action dated April 15, 2005. Claims 1, 5-7, 9-11 and 21 remain in this application. Claims 1 and 21 are the independent claims. Claims 1 and 21 have been amended. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Art-Based Rejections

Claims 1, 5-7, 10-11 and 21 were rejected under 35 USC §103(a) over USPN 6,169,323 (Sakamoto) in view of USPN 6,166,446 (Masaki); Claim 9 was rejected under 35 USC §103(a) over Sakamoto in view of Masaki and further in view of USPN 6,143,981 (Glenn). Applicant respectfully traverses these rejections and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

The Sakamoto Reference

Sakamoto is directed to a semiconductor device packaged in a plastic package having leads horizontally extending along the bottom surface of the plastic package. According to Sakamoto, the surface area for soldering is increased by making the end surface of a lead non-flat, uneven, pulsating, or saw-tooth shaped. (*See, Sakamoto, Col. 1, line 66 to Col. 2, line 21*).

The Masaki Reference

Masaki is directed to a resin-sealed type semiconductor device having a semiconductor element and electrodes. A radiator facilitates divergence of heat from the semiconductor element. A lead includes an inner lead portion and an outer

lead portion. A resin portion seals and embeds the semiconductor element. (*See, Masaki, Col. 1, lines 56-67*).

The Glenn Reference

Glenn is directed to plastic packages for housing an integrated circuit die and lead frames. According to Glenn, the package provides a rectangular metal lead frame with a substantially planar die pad positioned with and connected to the frame. A plurality of finger-like rectangular tabs extend from the frame toward the die pad without contacting the die pad. The die pad and tabs have peripheral side surfaces which include a reentrant portion(s) and asperities that enhance the connection of the die pad and tabs to the plastic encapsulating material. (*See, Glenn, Col. 1, line 57 to Col. 2, line 8*).

The Claims are Patentable Over the Cited References

The present invention is generally related to a semiconductor package technology including manufacture of a semiconductor device.

As defined by independent Claim 1, as amended, a semiconductor device includes a die pad, a semiconductor chip having an electrode and bonded to the die pad, and an inner lead having a sloping section sloping upward and outward, when a surface of the die pad which the semiconductor chip is bonded faces upward. A wire electrically connects the inner lead to the electrode. A sealing section seals the inner lead, the semiconductor chip, and the wire. An outer lead extends outward from the sealing section. The wire is bonded to the sloping section of the inner lead.

The applied references do not disclose or suggest the above features of the present invention as defined by amended independent Claim 1. In particular, the applied references do not disclose or suggest, "an inner lead having a sloping section sloping upward and outward, when a surface of the die pad which the semiconductor chip is bonded faces upward," as required by Claim 1.

Sakamoto is directed to a semiconductor device packaged in a plastic package having leads horizontally extending along the bottom surface of the plastic package. (*See, Sakamoto, Col. 1, line 66 to Col. 2, line 2*). Sakamoto discloses, in FIG. 4, a semiconductor device chip 2 electrically connected to leads 4 by means of bonding wires 3 and molded in a plastic mold 1. The leads 4 are arranged along the bottom surface of the plastic mold 1. (*See, Sakamoto, Col. 5, lines 36-40*). As shown in FIG. 4, Sakamoto specifically discloses leads 4 having a sloping section that slopes in a downward and outward direction from the upper surface of the die pad where the semiconductor device 2 is attached. The bonding wires 16 are bonded on the downward sloping section of the leads 4.

In contrast, the present invention specifically discloses, in FIG. 7, that the inner lead 42 has a sloping section 33 that slopes upward and outward from an upper surface of the die pad 14 when the die pad 14 faces upward. Independent Claim 1 has been amended to highlight this distinguishable feature of the present invention as indicated above. Even if the structure of Sakamoto was inverted so that the lead extended upward and outward, Sakamoto would still not teach each and every element of Claim 1, as amended, because after inversion, the die pad of Sakamoto would not be facing upward, but instead downward, which is different than the feature required in amended Claim 1. Therefore, independent Claim 1, as amended, clearly distinguishes over Sakamoto.

In the present invention, since the sloping section 33 of inner lead 42 slopes upward toward the outside of the semiconductor device 1, the end section of inner lead 42 may be disposed at a position lower than the electrode 12 of semiconductor chip 10. As a result, wire 16 may be bonded to inner lead 42 at a position lower than electrode 12 of chip 10. As shown in FIG. 7, the bonding position of the wire 16 and inner lead 42 may be lower than the electrode 12. The height of the loop of the wire 16 can be secured by allowing the bonding position of the wire 16 and the

inner lead 30 to be lower than the electrode 12. Therefore, the wire 16 can be prevented from coming in contact with an inner lead other than the target inner lead 42, whereby a highly reliable semiconductor device can be provided. The bonding position of wire 16 and inner lead 42 may be lower than the active surface of chip 10 on which electrode 12 is formed.

Sakamoto does not disclose or suggest each and every feature of the present invention as required by amended independent Claim 1, and the ancillary Masaki and Glenn references do not remedy the deficiencies of Sakamoto.

Therefore, since the applied references do not disclose or suggest the above features of the present invention as required by amended independent Claim 1, those references cannot be said to anticipate nor render obvious the invention which is the subject matter of amended independent Claim 1.

Accordingly, independent Claim 1, as amended, is believed to be in condition for allowance and such allowance is respectfully requested.

Independent Claim 21 has been amended to include similar subject matter as with Claim 1 and should be considered allowable for at least the same reasons as discussed above with reference to Claim 1.

The remaining Claims 5-7 and 9-11 depend either directly or indirectly from independent Claim 1 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references. Thus, the remaining Claims 5-7 and 9-11 are also believed to be in condition for allowance and such allowance is respectfully requested.

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Conclusion


In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

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By: 

Dariush G. Adli
Registration No. 51,386
Attorney for Applicant(s)